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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,176	09/24/2003	Chung-Che Tsai	MM4640	7002

7590 06/16/2005

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/671,176	TSAI, CHUNG-CHE	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *10-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable Admitted prior art, hereinafter APR (Figs. 4a-4f) in view of Jiang et al. (US 6208519), hereinafter Jiang and Shin et al, hereinafter Shin.

Regarding claim 1, Figs. 4a-4f of APR show a window ball grid array (WBGA) semiconductor package, comprising:

a substrate [10] having an upper surface and an opposite lower surface and having an opening [102] formed through the same;

at least one chip [11] mounted on the upper surface and over the opening of the substrate via an adhesive [12], and electrically connected to the lower surface of the substrate via a plurality of bonding wires [13] going through the opening, with gaps [G], not applied with the adhesive, being formed between the chip and the substrate;

a first molded encapsulation body [14, 15] made of a resin material and formed on the upper and lower surfaces of the substrate for encapsulating the chip and the bonding wires, wherein the gaps between the chip and the substrate allow the resin material to pass therethrough to fill the opening of the substrate and the gaps; and

a plurality of solder balls [16] bonded to area free of the second encapsulation body on the lower surface of the substrate and exposed outside.

Figs. 4a-4f of APR show the most aspect of the instant invention except "a second non-molded encapsulation body for covering the part of the first encapsulation body on the lower surface of the substrate; and a plurality of solder balls bonded to area free of the second encapsulation body on the lower surface of the substrate and exposed outside." Fig. 6 of Jiang shows a semiconductor device wherein a second encapsulation layer body [350] for covering the part of the first encapsulation body [160] on the lower surface of the substrate and a plurality of solder balls [123] bonded to area free of the second encapsulation body on the lower surface of the substrate and exposed outside.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Jiang into the device of APR in order to have a second encapsulation layer body for covering the part of the first encapsulation body on the lower surface of the substrate for an added protection of the recessed area, and to have a plurality of solder balls bonded to area free of the second encapsulation body on the lower surface of the substrate and exposed outside for an external connection.

The combined teachings of APR and Jiang show substantially the entire claimed structure except the second encapsulation body is non-molded. Shin discloses that encapsulation can be formed through dispensing method [col. 8, lines 42-49] or a printing method [col. 10, lines 25-31].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Shin into the device of APR and Jiang in order to have

the second encapsulation formed through non-molding process to accommodate a design specification.

Also, note that "non-molded" [not by a molding process] is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 2 and 3, Fig. 6 of Jiang shows the second encapsulation body [350] is on the lower surface of the substrate

Note that "is dispensed" and "is printed" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

In addition, Shin discloses the encapsulation body is dispensed on the lower surface of the substrate [col. 8, lines 42-49], or is printed on the lower surface of the substrate [col. 10, lines 25-31].

Regarding claim 4, Figs. 4a-4f of APR show the chip has an active surface and an opposite inactive surface, and the active surface faces the opening and is connected with the bonding wires, allowing the active surface to be entirely encapsulated by the adhesive and the first encapsulation body.

Regarding claim 6, Figs. 4a-4f of APR show the opening is of a rectangular shape having two opposite longer sides and two opposite shorter sides.

Regarding claim 7, Fig. 4a of APR shows the gaps between the chip and the substrate are located along the two shorter sides of the opening.

Regarding claims 8 and 9, Figs. 4a-4f of APR show the gaps have a height equal to a thickness of the adhesive which is predetermined to allow particles of the resin material to pass through the gaps. In addition, it is obvious that the gaps in the device of APR have a height equal to a thickness of the adhesive since the gap is formed where the adhesive is not applied.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable Huang et al. (US 6528722) hereinafter Huang in view of Jiang et al. (US 6208519), hereinafter Jiang and Shin et al, hereinafter Shin.

Regarding claim 1, Fig. 1 of Huang shows a window ball grid array (WBGA) semiconductor package, comprising:

a substrate [52] having an upper surface[525] and an opposite lower surface[524] and having an opening formed through the same;

at least one chip [53] mounted on the upper surface and over the opening of the substrate via an adhesive [57], and electrically connected to the lower surface of the substrate via a plurality of bonding wires [54] going through the opening, with gaps, not applied with the adhesive, being formed between the chip and the substrate;

a first molded encapsulation body [55] made of a resin material and formed on the upper and lower surfaces of the substrate for encapsulating the chip and the bonding wires, wherein the gaps between the chip and the substrate allow the resin material to pass therethrough to fill the opening of the substrate and the gaps; and

a plurality of solder balls [56] bonded to area free of the second encapsulation body on the lower surface of the substrate and exposed outside.

Fig. 1 of Huang shows the most aspect of the instant invention except "a second non-molded encapsulation body for covering the part of the first encapsulation body on the lower surface of the substrate; and a plurality of solder balls bonded to area free of the second encapsulation body on the lower surface of the substrate and exposed outside." Fig. 6 of Jiang shows a semiconductor device wherein a second encapsulation layer body [350] for covering the part of the first encapsulation body [160] on the lower surface of the substrate and a plurality of solder balls [123] bonded to area free of the second encapsulation body on the lower surface of the substrate and exposed outside.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Jiang into the device of Huang in order to have a second encapsulation layer body for covering the part of the first encapsulation body on the lower surface of the substrate for an added protection of the recessed area, and to have a plurality of solder balls bonded to area free of the second encapsulation body on the lower surface of the substrate and exposed outside for an external connection.

The combined teachings of Huang and Jiang show substantially the entire claimed structure except the second encapsulation body is non-molded. Shin discloses that encapsulation can be formed through dispensing method [col. 8, lines 42-49] or a printing method [col. 10, lines 25-31].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Shin into the device of Huang and Jiang in order to have the second encapsulation formed through non-molding process to accommodate a design specification.

Also, note that "non-molded" [not by a molding process] is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 2 and 3, Fig. 6 of Jiang shows the second encapsulation body [350] is on the lower surface of the substrate

Note that "is dispensed" and "is printed" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

In addition, Shin discloses the encapsulation body is dispensed on the lower surface of the substrate [col. 8, lines 42-49], or is printed on the lower surface of the substrate [col. 10, lines 25-31].

Regarding claim 4, Fig. 1 of Huang shows the chip has an active surface and an opposite inactive surface, and the active surface faces the opening and is connected with the bonding wires, allowing the active surface to be entirely encapsulated by the adhesive and the first encapsulation body.

Regarding claim 5, Fig. 8 of Huang shows the inactive surface of the chip is exposed to outside of the first encapsulation body.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Stephen Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

Steven Loke
Primary Examiner